GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS AND COMMUNICATION ENGINEERING

TESTING AND VERIFICATION

SUBJECT CODE: 2181107

B.E. 8th SEMESTER

Type of course: Introductory course for VLSI testing

Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, and various techniques for test pattern generation etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks			Practical Marks			
L	T	P	C	ESE (E)	PA (M)		PA (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	150

Content:

Sr No	Course Content	Teaching hours	Module weightage
1	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	**8**	**15%**
2	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability	**14**	**30%**
3	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation	**10**	**20%**
4	**Verification:** Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages	**8**	**15 %**
5	**Functional Verification:** Introduction to test bench, Test bench architecture, Types of test benches, case study	**12**	**20 %**
Total		**52**	

Reference Books:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001
6. Janick Bergeron, Writing Testbenches, Functional Verification of HDL Models, Springer

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10	**15**	**15**	**15**	**15**	**0**

Course Outcome:

1	To realize importance and challenges of VLSI Testing at different abstraction levels.
2	To study and apply various fault models for generation of test vectors.
3	To calculate observability and controllability parameters of given circuit.
4	To study techniques to improve testability of a given circuit.
5	To convert a given circuit into a scan design.
6	To apply concepts of logic simulation and fault simulation in designing and testing of VLSI circuits.
7	To identify the different characteristics of verification, and apply different verification methods.

Suggested List of Experiments:

1	Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
2	Write a VHDL/Verilog code to realize functioning of control Point Insertion technique.
3	Write VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered muxed-D scan cell.
4	Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
5	Write a VHDL/Verilog code to realize functioning of LSSD double latch design
6	Write a VHDL/Verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain
7	Write a VHDL/Verilog code to realize functioning of Fixing bus contention in scan design rules.
8	Write a VHDL/Verilog code to realize functioning of Adding a lock-up latch between cross-clock-domain scan cells.
9	To develop an exhaustive test bench for lower level combinational designs: 1. Adder and 2. multiplexer.
10	To develop an exhaustive test bench for J-K flip-flop.
11	To develop an exhaustive test bench for 4 bit up-down counter.
12	To verify an 8 bit shift register.
13	To prepare a complete test vector set for all possible stuck at faults parity checker where the

data word is of 2 bit.

Suggested Open Ended Problems:

1 Write a C program to calculate observability and controllability parameters of given circuit.
2 Write a C program to generate test vectors for stuck at faults for a given combinational circuit.
3 Write a C program to generate test vectors for transistors faults for a given circuit.

List of Open Source Software/ Learning website:

1. ngspice/xilinx (software)
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu

ACTIVE LEARNING ASSIGNMENTS: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.