GUJARAT TECHNOLOGICAL UNIVERSITY

COMPUTER ENGINEERING (07) AND INFORMATION TECHNOLOGY (16)
EMBEDDED & VLSI DESIGN
SUBJECT CODE: 2160709
B.E. 6thSEMESTER

Type of course: Elective

Prerequisite: NA

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks			Practical Marks			
				ESE (E)	PA (M)		ESE (V)		PA (I)	
					PA	ALA	ESE	OEP		
4	0	2	6	70	20	10	20	10	20	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Introduction to Embedded Systems** History of embedded systems, Classification of embedded systems, Major application area of embedded systems, Purpose of embedded systems, Fundamental issues in hardware software co-design, Introduction to unified modeling language (UML)	06	15
2	**Typical Embedded Systems** Core of the Embedded Systems, Memory, Sensors and actuators, Communication interface, Embedded firmware	10	15
3	**Embedded product development life cycle** Product enclosure design tool, Product enclosure development techniques, Objective of EDLC, Different phases of EDLC and approaches	8	10
4	Introduction and fabrication of MOSFET VLSI Design Flow, Design hierarchy, Design Methodology, nMOS,pMOS,CMOS fabrication process	4	10
5	MOS Transistor Metal Oxide Semiconductor (MOS) structure, The MOS System under external Structure &Operation of MOS transistor, MOSFET Current-Voltage characteristics Introduction, Resistive load Inverter Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load) CMOS Inverter	12	20
6	MOS combinational, sequential and dynamic logic circuits Introduction, MOS logic circuits with Depletion nMOS Loads CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (Tgs) Introduction, Behaviour of Bistable elements, The SR latch circuit Clocked latch & Flip-flop circuit, CMOS D-latch & Edge-triggered flip-	8	15

	flop		
7	Chip input and output On chip Clock Generation and Distribution Latch –Up and its Prevention	4	5
8	Design for testability Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques	4	10

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
20	**15**	**15**	**10**	**10**	**05**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Introduction to Embedded Systems by shibu K V mcgraw hill
2. System Design: A Unified Hardware/Software Introduction by Frank Vahid and Tony D. Givargis, Addison Wesley, 2002.
3. Sung-Mo-Kang, UsufLeblebici ,CMOS digital integrated circuits: Analysis and Design, Tata McGrawhill,2003
4. Douglas Pucknell, Basic VLSI Design,PHI, 1999
5. The AVR microcontroller and Embedded Systems by muhammad Ali Mazidi, Sarmad Naimi, Sepehr Naimi
6. Computers as Components by Wayne Wolf, Morgan Kaufmann, 2001
7. Embedded C programming and the ATMEL AVR by Barnett, cox and o'cull, Thomson
8. Wayne Wolf ,Modern VLSI Design., Person Education, 2001
9. John Uyemura ,Introduction to VLSI circuits and systems, Wiley, 2002

Course Outcome:

After completion of the course students will be able to

1. Will learn various peripheral components.
2. Use AVR Programming to interface various peripherals.
3. Able to visualize the design of an embedded system to unified modeling language.
4. Able to analyze and document various development cycle for the embedded system

List of Experiments:

1. Flash/toggle/on-off single LED.
2. Alternate ON-OFF eight LEDs.
3. Display 0 to 9 on segment
4. Multiplexed 4 7-segment & do following:
   IfSW1 press, display 0 to 9

If SW2 press, display 00 to 99
If SW3 press, display 000 to 999
If SW4 press, display 0000 to 9999

5. Transmit “Hello World!” serially and display on monitor and Transmit and receive the data in serially
6. Display the string on LCDEx.; “Hello World” and Display the string on LCD using 4 pin Ex.; “Hello World”
7. Press any key from 4*4 keypad and display on LCD. And Assume one password is stored in system. Enter password using keypad and Check whether is correct or wrong and display status on LCD
8. To implement all logic gates using VHDL.
9. To implement all logic gates using behavioral method
10. To implement eight different logic gates with the help of 3-bit selection line.
11. To implement all flip-flops (s-r, j-k, t, d) using.
12. To implement half adder with data flow, structural and behavioral method.
13. To implement full-adder with data flow, structural and behavioral method.
14. To implement 8:1 multiplexer.
15. To implement 2:4 line decoder.
16. To implement 4-bit adder.
17. To implement 4-bit comparator.
18. To implement BCD to 7-segment decoder using VHDL
19. To design sequence detector (a) Mealy model (b) Moore model

Design based Problems (DP)/Open Ended Problem:

VHDL/Verilog based mini project with emphasis on design and implementation is Compulsory:

Design small processing element using VHDL/Verilog Hardware description having adders, subtractions, and multiplying operations with counting facility

ACTIVE LEARNING ASSIGNMENTS: Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to GTU.