GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT

Course Curriculum

DIGITAL LOGIC DESIGN
(Code: 3331104)

Diploma Programme in which this course is offered	Semester in which offered
Electronics and Communication Engineering	3rd Semester

1. RATIONALE

Digital technology is the fastest growing technology and have revolutionised the electronics Industry. In most of the applications digital technology has replaced analogue technology. Digital logic is heart of digital electronic circuits. A basic understanding of this subject is therefore essential to effectively maintain digital electronic devices. The study of this course will enable the students to test the working and rectify the faults of common digital circuits.

2. COMPETENCY (Programme outcome according to NBA Terminology)

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competency:

- **Maintain the digital electronic circuits.**

3. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	ESE	PA	ESE	PA	
03	01	02	06	70	30	30	20	150

Legends: L - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** - Practical; **C** - Credit; **ESE** - End Semester Examination; **PA** - Progressive Assessment

4. COURSE DETAILS

Unit	Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology)	Topics and Sub-topics
Unit – I Number systems and codes	1a.Differentiate binary and decimal number system 1b. Perform arithmetic operations on Binary numbers	1.1 Introduction to Digital System 1.2 Binary and digital number system. 1.3 Binary arithmetic operations: addition, subtraction, multiplication and division 1.4 Complements: n's, (n-1)'s compliments 1.5 Subtraction using complement method.
	1c. Convert of number systems to octal to hexadecimal and vice versa	1.6 Octal number system 1.7 Hexadecimal number system. 1.8 Conversion from binary to octal, decimal and hexadecimal number systems and vice versa.
	1d. Interpret the Binary codes.	1.9 Codes: BCD, Gray, Excess-3, ASCII, EBCDIC.
Unit – II Boolean algebra and logic gates	2a. Simplify the Boolean functions.	2.1. Basic theorems and properties of Boolean algebra. 2.2. Boolean functions: Sum of Product (SOP) and Product of Sum (POS) expressions.
	2b.Describe functions of Logic gates.	2.3. Basic Digital Logic Gates: Symbol, operation and truth-table of AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR gates. 2.4. Positive and negative logic system.
	2c. Implement the Boolean functions using logic gates for	2.5. Algebraic simplification of Boolean expression 2.6. NAND-NOR circuit implementations 2.7. AND-OR -**Invert** implementations
	2d.Simplify Boolean expression using K-map.	2.8. Karnaugh map(K-map) simplification Techniques for SOP and POS functions up to Four variable 2.9. Don't care condition for simplification of Boolan function.
Unit – III Combinational logic circuits	3a. Explain function of combinational circuits	3.1. Combinational Circuits: Half adder, full adder, parallel binary adder, half Subtractor , full subtractor, parallel binary subtractor,1's complement subtractor, 2's complement subtractor/adder BCD adder.
	3b. Implement various combinational circuits.	3.2. Binary to Gray and Gray to binary code converters 3.3. Decoder and Encoder 3.4. Multiplexers and Demultiplexers 3.5. Magnitude Comparator 3.6. Bit error correction: Parity Generators and Checkers. 3.7. BCD to Seven segment decoder

Unit	Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology)	Topics and Sub-topics
Unit – IV Sequential logic circuits	4a. Describe the function of various types of flip-flops with the help of circuit diagram, truth table and timing diagram.	4.1. Types of flip-flops: Latch and Flip-flop, S-R flip-flops, asynchronous and synchronous S R flip flops, D flip flop, J-K flip flop, JK master slave flip flop, T Flip Flop, Edge triggered Flip-Flops.
	4b. Describe the working of various Registers with the help of circuit diagram, truth table and timing diagram.	4.2. Registers: Classification of Shift Register, Serial in serial-out, serial-in parallel-out, parallel-in serial-out and parallel-in parallel out.
	4c. Explain the working of various types of Counters with the help of circuit diagram, truth table and timing diagram.	4.2. Asynchronous(ripple) 4-bit binary counter 4.3. BCD Counter. 4.4. Synchronous counters 4.5. UP/DOWN counter 4.6. Ring counters.
Unit – V D/A,A/D and Memories	5a. Explain working of D/A converters 5b. Explain working of A/D converters.	5.1. D/A Conversion: Weighted resister, R-2R ladder network, Accuracy and Resolution. 5.2. A/D Conversion: Dual slope type, Counter type, Successive approximation, Flash type.
	5c. Classify semiconductor Memories	5.3. Semiconductor Memory: RAM-SRAM and DRAM, ROM-PROM, EPROM, EEPROM, Flash memory.
Unit – VI Digital Integrated Circuits	6a. Explain working of Bipolar and unipolar logic families with their characteristics.	6.1. Logic families and level of Integration SSI, MSI,L SI, VLSI 6.2. Characteristics of digital ICs-fan-in, fan-out, propagation delay, power dissipation, noise margins, figure of merit. 6.3. Transistor-Transistor logic (TTL) circuits: Open collector output, Totem pole output, Tri-state output. 6.4. Emitter Coupled Logic (ECL). 6.5. Integrated Injection Logic (IIL). 6.6. MOS and CMOS Logic.
	6b. Compare Logic families.	6.7. Comparison of different logic families
	6c. Define programmable Devices.	6.8. Programmable devices : PLA,PLD,PAL,FPGA,ASIC

5. SUGGESTED SPECIFICATION TABLE WITH HOURS and MARKS (THEORY)

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number systems and codes	06	02	04	03	09
II	Boolean algebra and logic gates	08	00	08	06	14
III	Combinational logic circuits	08	04	06	04	14
IV	Sequential logic circuits	08	04	06	04	14
V	D/A,A/D and Memories	06	04	04	02	10
VI	Digital Integrated Circuits	06	04	05	00	09
Total		**42**	**18**	**33**	**19**	**70**

Legends: R = Remember; U = Understand; A = Apply and above levels (Bloom's revised taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

6. SUGGESTED LIST OF EXERCISES/PRACTICAL

The practical/exercises should be properly designed and implemented with an attempt to develop different types of practical skills (**Course Outcomes in psychomotor and affective domain**) so that students are able to acquire the competencies (Programme Outcomes). Following is the list of practical exercises for guidance.

Note: Here only course outcomes in psychomotor domain are listed as practical/exercises. However, if these practical/exercises are completed appropriately, they would also lead to development of Programme Outcomes/Course Outcomes in ***affective domain*** as given in a common list at the beginning of curriculum document for this programme. Faculty should refer to that common list and should ensure that students also acquire those Programme Outcomes/Course Outcomes related to affective domain.

S. No.	Unit No.	Practical/Exercise ('Course Outcomes' in Psychomotor Domain according to NBA terminology)	Approx Hrs. Required
01.	II	Build/Test the functionality of Basic and Advance Logic Gates**.**	2
02.	II	Build/Test 2 input basic logic gates using NAND gate .	2
03.	II	Build/Test 2 input basic logic gates using NOR gate .	2
04.	III	Build a circuit to Convert 4 bit Binary to Gray Code using logic gates	2
05.	III	Build a circuit to Convert 4 bit Gray to Binary Code using logic gates	2
06.	III	Build/Test Half Adder Circuit.	2
07.	III	Build/Test Full Adder Circuit.	2
08.	III	Build/Test Half Subtractor Circuit.	2
09.	III	Build/Test 4 bit Parallel Adder circuit.	2
10.	III	Build/Test the 3X8 Decoder circuit.	2
11.	III	Build/Test the 8X1Multiplexer circuit.	2

S. No.	Unit No.	Practical/Exercise ('Course Outcomes' in Psychomotor Domain according to NBA terminology)	Approx Hrs. Required
12.	III	Build/Test BCD to Seven segment LED Display circuit.	2
13.	IV	Build/Test the functionality of the SR Flip-Flop.	2
14.	IV	Build/Test the functionality of the JK Flip-Flop.	2
15.	IV	Build/Test the working of the Shift Register.	2
16.	IV	Build/Test the working of the 4 bit Ripple Counter.	2
17.	IV	Build/Test the working of 4 bit UP - DOWN Counter.	2
18.	V	Build/Test Analog/Digital converter (ADC 0809 or equivalent)	2
19.	V	Build/Test digital to analog converter (DAC 0808 or equivalent).	2
20.	VI	Design and Develop mini project using digital logic.	2
		Total	**40**

7. SUGGESTED LIST OF STUDENT ACTIVITIES

i. Read and note down specifications of Digital ICs using data sheet: IC number/ Pin Diagram/voltage levels, applications for the following Digital ICs (TTL/CMOS): AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR gates, Decoder, Multiplexer, BCD to 7-segment decoder, SR FF,JK FF, D FF, shift Register, Counter, ADC, DAC.
ii. Solve real life problems using binary logic theory and implement it using digital logic circuits.
iii. Explore working of Digital clock/Digital panel.
iv. Prepare mini project using Various Digital IC and display devices.

8. SPECIAL INSTRUCTIONAL STRATEGIES (if any)

i. Take small instrumentation components to the class when teaching
ii. Use tutorial classes for designing simple digital logical circuits and other teacher guided student activities.
iii. Internet based home assignments
iv. Mini projects (in group of three to four students)

9. SUGGESTED LEARNING RESOURCES

A) List of Books

S. No.	Title of Books	Author	Publication
1.	Digital Logic and Computer Design	M. Morris Mano	Pearson Education, New Delhi, 2011 or latest
2.	Digital Principles and Application	Malvino and Leech	TMH Pub., New Delhi, 6th Edition or latest
3.	Fundamentals of Digital Circuits	A. Anand Kumar	PHI Learning, New Delhi, 2nd Edition or latest
4.	Morden Digital Electronics	Jain, R P	TMH Education , New Delhi, 3rd Edition or latest
5.	Digital Electronics	Kharate G.K.	OXFORD University Press, 2010

B) List of Major Equipment/Materials with Broad Specifications

i. Digital Logic trainer board.
ii. A/D and D/A trainer modules.
iii. Universal counter module
iv. Digital IC tester
v. Regulated power supply

C List of Software/Learning Websites

i. www.nptel.iitm.ac.in
ii. www.ocw.mit.edu
iii. www.slideshare.net/

10. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- **Prof. K. R .Vadalia**, Lecturer Electronics and Comm. Engineering, G.P. Rajkot.
- **Prof. T. P. Chanpura**, Lecturer Electronics and Comm. Engineering, G.P. Ahmedabad.
- **Prof. M. S. Dave**, Lecturer Electronics and Comm. Engineering, G.P. Ahmedabad.
- **Prof. U .V. Buch**, Lecturer Electronics and Comm. Engineering, G.P. Gandhinagar
- **Prof. K. A. Dave**, Lecturer Electronics and Comm. Engineering, VPMP, Gandhinagar

Coordinator and Faculty Members from NITTTR Bhopal

- **Dr. Anjali Potnis**, Associate Professor, Department of Electrical and Electronics Engineering,
- **Dr. Joshua Earnest**, Professor, Department of Electrical and Electronics Engineering,